

31050 U.S. PTO
10/092310



U.S. UTILITY Patent Application

PATENT NUMBER and
ISSUE DATE

APPL NUM 10092310	FILING DATE 03/07/2002	CLASS 430	SUBCLASS 27	GAU 1752	EXAMINER W. J. R. H.
----------------------	---------------------------	--------------	----------------	-------------	-------------------------

**APPLICANTS: Ooturo Akihiko; Takechi Satoshi;

**CONTINUING DATA VERIFIED: *None*

BEST AVAILABLE COPY

** FOREIGN APPLICATIONS VERIFIED: *None*
JAPAN 2001-180584 06/14/2001

PG-PUB DO NOT PUBLISH ☐

RESCIND ☐

Foreign priority claimed

☒ yes ☐ no

35 USC 119 conditions met

☒ yes ☐ no

Verified and Acknowledged Examiners's initials

[Signature]

ATTORNEY DOCKET NO

020201

TITLE: Multi-layered resist structure and manufacturing method of semiconductor device

U.S. DEPT. OF COMM./PAT. & TM. PTO-436L (Rev. 12-94)

NOTICE OF ALLOWANCE MAILED		Assistant Examiner	CLAIMS ALLOWED	
			Total Claims	Print Claim for O.G.
ISSUE FEE		Primary Examiner	DRAWING	
Amount Due	Date Paid		Sheets Drawg.	Figs. Drawg.
<input type="checkbox"/> TERMINAL DISCLAIMER		PREPARED FOR ISSUE	Application Examiner	
<p>WARNING: The information disclosed herein may be restricted. Unauthorized disclosure may be prohibited by the United States Code Title 35, Sections 122, 181 and 368, Possession outside the U.S. Patent & Trademark Office is restricted to authorized employees and contractors only.</p>				

FILED WITH:

☐ DISK (CRF)

☐ CD-ROM

(Attached in pocket on right inside flap)